# WEST Search History

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DATE: Wednesday, November 24, 2004

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| ☐ | L83 | (cpu or processor) with L82 | 3 |
| ☐ | L82 | 114 with (fpga or pld) | 52 |
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| ☐ | L79 | 114 with (programmable gate$1 or programmable logic) | 184 |
| ☐ | L78 | L77 not (165 or 163 or 161 or 160 or 158 or 170 or 175) | 220 |
| ☐ | L77 | processor with 174 | 265 |
| ☐ | L76 | L75 not (165 or 163 or 161 or 160 or 158 or 170) | 2 |
| ☐ | L75 | cpu same L74 | 36 |
| ☐ | L74 | 115 with (programmable gate$1 or programmable logic) | 1202 |
| ☐ | L73 | L70 not (165 or 163 or 161 or 160 or 158) | 14 |
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| ☐ | L70 | cpu same L69 | 22 |
| ☐ | L69 | 115 with (fpga or pld) | 572 |
| ☐ | L68 | 115 same (fpga or pld) | 1225 |
| | *DB=USPT,USOC; PLUR=NO; OP=ADJ* | | |
| ☐ | L67 | L66 not (165 or 163 or 161 or 160 or 158) | 37 |
| ☐ | L66 | processor with 159 | 80 |
| ☐ | L65 | processor with 162 | 42 |
| ☐ | L64 | processor same 162 | 67 |
| ☐ | L63 | core same L62 | 14 |
| ☐ | L62 | 115 with (fpga or pld) | 141 |
| ☐ | L61 | L60 not 158 | 17 |
| ☐ | L60 | cpu same L59 | 23 |
| ☐ | L59 | 115 with (programmable gate$1 or programmable logic) | 413 |
| ☐ | L58 | cpu same L57 | 16 |
| ☐ | L57 | 115 same (fpga or pld) | 327 |
| ☐ | L56 | cpu and L55 | 356 |
| ☐ | L55 | 115 and (fpga or pld) | 985 |

| | | | |
|---|---|---|---|
| ☐ | L54 | logic integrated circuit$1 and l22 | 0 |
| ☐ | L53 | l22 and (programmable gate$1 or programmable logic) | 0 |
| ☐ | L52 | l22 and (fpga or pld) | 0 |
| ☐ | L51 | enabl$3 and (L2 or L6) | 2 |
| ☐ | L50 | enabl$3 and L49 | 1 |
| ☐ | L49 | (L2 or L6) and programmable | 1 |
| ☐ | L48 | (L2 or L6) and logic | 2 |
| ☐ | L47 | L2 or L6 and logic | 2 |
| ☐ | L46 | cpu with L44 | 4 |
| ☐ | L45 | reprogram$4 with L44 | 4 |
| ☐ | L44 | fpga with (simulat$3 or emulat$3) | 299 |
| | *DB=EPAB,JPAB,DWPI,TDBD; PLUR=NO; OP=ADJ* | | |
| ☐ | L43 | reprogram$4 with L42 | 0 |
| ☐ | L42 | fpga with (simulat$3 or emulat$3) | 79 |
| ☐ | L41 | fpga simulator | 0 |
| | *DB=USPT; PLUR=NO; OP=ADJ* | | |
| ☐ | L40 | US-6260172-B1.did. | 1 |
| ☐ | L39 | US-6089460-A.did. | 1 |
| ☐ | L38 | US-6260172-B1.did. | 1 |
| | *DB=PGPB; PLUR=NO; OP=ADJ* | | |
| ☐ | L37 | US-20010011214-A1.did. | 1 |
| ☐ | L36 | US-20010011214-A1.did. | 1 |
| | *DB=EPAB,JPAB,DWPI,TDBD; PLUR=NO; OP=ADJ* | | |
| ☐ | L35 | cpu and L34 | 11 |
| ☐ | L34 | logic integrated circuit$1 | 904 |
| | *DB=PGPB,USPT; PLUR=NO; OP=ADJ* | | |
| ☐ | L33 | 5968161.uref. | 6 |
| ☐ | L32 | altera.as. and L31 | 1 |
| ☐ | L31 | fpga same cpu | 1147 |
| ☐ | L30 | altera.as. and cpu | 186 |
| | *DB=USPT; PLUR=NO; OP=ADJ* | | |
| ☐ | L29 | cpu and L27 | 35 |
| ☐ | L28 | cpu core$1 and L27 | 0 |
| ☐ | L27 | L26 and L15 | 116 |
| ☐ | L26 | L12.ti,ab,clm. | 1427 |
| ☐ | L25 | 5933642.pn. | 1 |
| | *DB=EPAB,JPAB,DWPI,TDBD; PLUR=NO; OP=ADJ* | | |
| ☐ | L24 | 5933642.pn. | 1 |

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|---|---|---|---|
| ☐ | L23 | L20 and L22 | 2 |
| ☐ | L22 | firmware or nanoinstruction$1 or nano-instruction$1 or nanocode or nano-code or nanoprogram or nano-program or L21 | 15749 |
| ☐ | L21 | microinstruction$1 or micro-instruction$1 or microcode or micro-code or micro-operation$1 or microoperation$1 or micro-op$1 or microop$1 or micro-program$1 or microprogram$1 | 11222 |
| ☐ | L20 | cpu and L19 | 196 |
| ☐ | L19 | field programmable gate array$1 or fpga$1 | 3251 |
| | *DB=PGPB,USPT; PLUR=NO; OP=ADJ* | | |
| ☐ | L18 | cpu core$1 and L17 | 12 |
| ☐ | L17 | L12 same L15 | 1418 |
| ☐ | L16 | L13 and L15 | 92 |
| | *DB=USPT,PGPB; PLUR=NO; OP=ADJ* | | |
| ☐ | L15 | firmware or nanoinstruction$1 or nano-instruction$1 or nanocode or nano-code or nanoprogram or nano-program or L14 | 52363 |
| ☐ | L14 | microinstruction$1 or micro-instruction$1 or microcode or micro-code or micro-operation$1 or microoperation$1 or micro-op$1 or microop$1 or micro-program$1 or microprogram$1 | 14283 |
| | *DB=PGPB,USPT; PLUR=NO; OP=ADJ* | | |
| ☐ | L13 | cpu core$1 and L12 | 135 |
| ☐ | L12 | field programmable gate array$1 or fpga$1 | 16012 |
| ☐ | L11 | L9 and core | 2737 |
| ☐ | L10 | (L2 or L6) and L9 | 0 |
| ☐ | L9 | field programmable gate array$1 | 12350 |
| ☐ | L8 | (L2 or L6) and fpga | 0 |
| ☐ | L7 | (L2 or L6) and core | 0 |
| ☐ | L6 | 5675777.pn. | 1 |
| ☐ | L5 | glickman.in. and jeff.in. | 6 |
| ☐ | L4 | glickman.in. and taraplex.as. | 0 |
| ☐ | L3 | glickman.in. and teraplex.as. | 0 |
| ☐ | L2 | 6389528.pn. | 1 |
| ☐ | L1 | pappalardo.in. and tesi.in. | 7 |

END OF SEARCH HISTORY